Low Power And High Performance Current Steering DAC Using Different GDI Logics

G.Maheswara Murthy[1], B.Srinivas[2]

[1](PG Scholar, ECE Department, MVGR College of Engineering, INDIA)
[2](Assistant Professor, ECE Department, MVGR College of Engineering, INDIA)
Corresponding Author: G.Maheswara Murthy

Abstract: *The current steering digital-to-analog converters (DAC) carry out a vital role in data-processing systems like communication systems. Digital-to-analog (DAC) converters used in modern communication systems mainly for linearity, effectiveness, and for high speed applications. The segmented approach of DAC in proposed work is mainly used for minimizing power dissipation, chip area. In general DAC have a tendency to operate at high rate of sampling, the current switches will affect the output with glitches because the transitions made at high sampling rate. In digital-to-analog converters decoders are designed with conventional CMOS logic, which are having more power dissipation, chip area than the proposed Gate Diffusion (GDI) Input logics. In this paper to minimize the power dissipation of decoder circuit in DAC, binary-thermometer decoder is implemented with GDI, Full-swing (FSGDI) and Transmission (TSGDI) logics. This method has been successfully shown for 8-bit 500-MHz segmented-current steering DAC having a less number of transistors, which results in low power dissipation.*

Keywords - *Binary to Thermometer decoder, Current-Steering DAC, FSGDI, GDI Logic, TSGDI.*

I   Introduction

In modern communication systems like GSM, need high speed and linearity DAC to integrate both analog and digital circuits on a single chip. Among the other types of DACs [1] for example R (resistor)-string [2], RC-hybrid and, Current steering DAC (CSDAC) etc. CSDAC is mostly chosen because of the compatibility with CMOS Design process.

Binary weighted architecture is simple to construct and easy to control the logic, as it uses the binary code as input to control the switching of current sources, excluding any requirement of decode logic. In binary-weighted type of architecture performance is degraded by the glitches, due to current source mismatches and the swing between large numbers of inputs. For example the swing between the input code 0110 and 1000 shows that the required current sources to be on at 1000 is higher than current sources required for 0110 here the mismatch between current sources occurs.

The segmented decoder [3] structure used to gain high performance in digital to analog converters. The segmented decoder structure reduces the number of transistors required for the decoder circuit, which results in a diminution in the chip area of DAC. The thermometer code architecture is unary weighted architecture, which uses a single weighted current source. For example, consider a two bit thermometer decoder; it uses three same weighted current sources controlled by thermometer decoder outputs. The segmented decoder [1] structure uses both binary weighted, unary weighted structures. Binary weighted decoder architecture uses more current sources, so in order to reduce the number of current sources; segmented structure is used in place of binary weighted structure. In segmented structure, at LSB's (Least Significant Bit) binary weighted current sources were used and at MSB's (Most Significant Bit), unary weighted current sources were used by using this type of structure the area and power dissipation both are reduced.

The conventional CMOS (Complementary Metal Oxide Semiconductor) logic is used in the design of electronic circuits. Nowadays the circuits need to be compatible with regular needs like minimized chip area and low power dissipation. To convince those needs the micron technology is reduced to 22nm technology. Here again a tradeoff between threshold voltage and channel length is rising because of decrease in channel length. One of the sub-thresholding techniques for lowering power, chip area are GDI (Gate Diffusion input) logics [4]. In GDI logic the inputs are applied at the both gates of NMOS and PMOS, source terminal of NMOS, drain terminal of PMOS transistors. The GDI logic can't give full swing output signal. The Full Swing GDI logic (FSGDI), Transmission gate GDI Logic (TSGDI) logics gives the improved swing of output signal.

II   Digital To Analog Converter

A Digital to Analog Converter is used in communication systems to convert the digital data in to analog data. It is an important sub-system in communication system, because the data is decoded from the received data which is the digital form. The received digitized data is in form of quantized voltage levels it needs to decode the data with respect to those levels in form of analog signal. In DAC the main circuitry which controls the logic is decoder circuit and then the current sources are used for constructions of analog signal. The binary weighted tree decoder type architecture uses more area, because of more logic is needed. The binary weighted tree decoder type architecture uses more area, because of more logic is needed. The R-2R ladder circuit DAC [2] is a best example of binary weighted DAC, which uses the cascading R-2R structure repeatedly. Here, in this type of DACs the mismatch between the circuitry is less due to the equal valued components spread over the circuit which improves precision of the output. But the chip area required to manufacture these types of DACs is more. The oversampling converters are mainly used for pulse modulation techniques and also these types of DACs are used for low resolution applications. Hybrid DACs [1] are most commonly using in recent applications, because these types of DACs used both the unary and binary weighted principles while designing the DAC. In this proposed work the decoder circuit is designed with thermometer code principle, which means that the Binary-Thermometer (BT) decoder logic used in this paper.
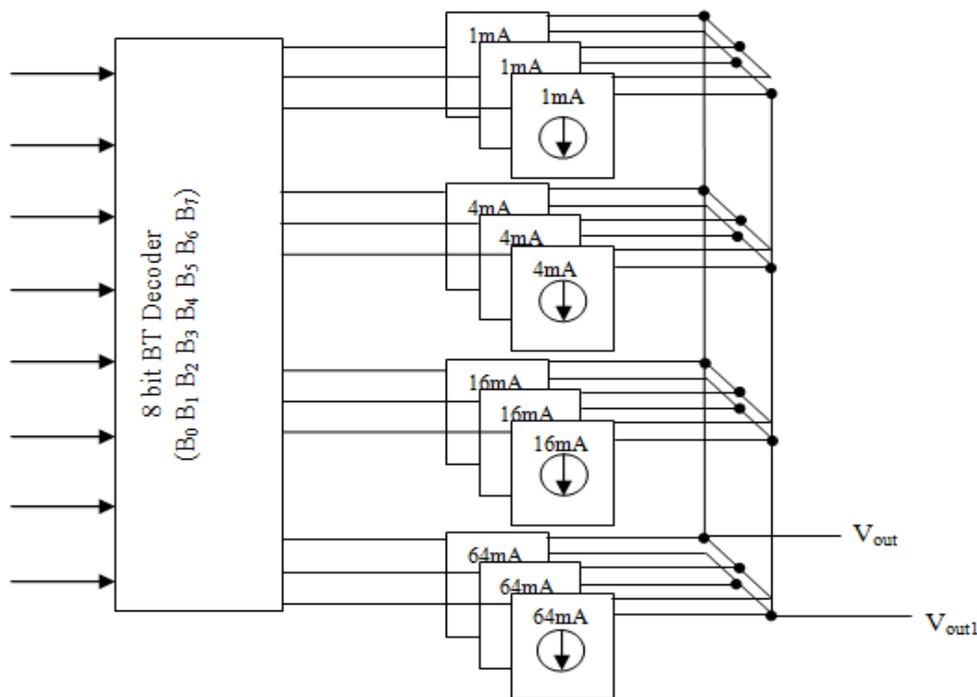
Fig. 1 8-bit Current steering DAC

2.1. Construction and Segmentation of proposed DAC:

The precise information regarding the segmentation of 8 bit DAC is specified in this section. In Current steering DACs segmentation is applied to input bits to reduce the chip area and power dissipation. The segmentation is applied in different ways on LSBs and MSBs. This paper is proposed for low chip area and low power dissipation; so the control logic which controls the unary weighted current cells is reduced. Which means the numbers of output signals from the decoder circuit is reduced. In a decoder circuit the number of outputs is based on number of inputs, if N number of inputs were applied to the decoder circuit then 2^{N-1} outputs will obtain at output. For example, 8 (N) bit input is applied at the input section then 256 ($2^{8-1} \Rightarrow 2^7$) outputs are obtained at the output, which are nothing but the 256 (0-255) control signals. To reduce the control signals the proposed decoder of 8 bits is divided into four sub-groups of two bit BT decoders. Therefore, each one of two bit BT decoder controls three current sources of same weights. The proposed BT decoder circuit of 2 bit is shown in figure blow. By using four 2 bit BT decoders [5], proposed 8 bit BT decoder circuit is constructed.

Binary code		Thermometer code		
B_1	B_0	T_3	T_2	T_1
0	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	1	1	1
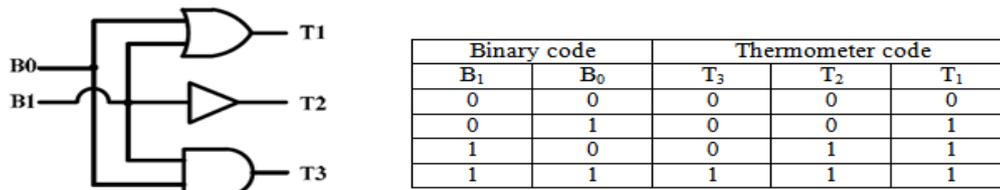
Fig.2 2-Bit BT Decoder and its operating procedure

The conventional CMOS logic used to construct the decoder circuit occupies more space and power dissipation also high. In this paper GDI logics [4] were used to construct the decoder circuit. 2 bit BT decoder uses one AND gate, one OR gate, and one buffer circuit. These are implemented in GDI, FSGDI, TSGDI logics and the resulting power dissipation and area of respective logics were given in the below table.
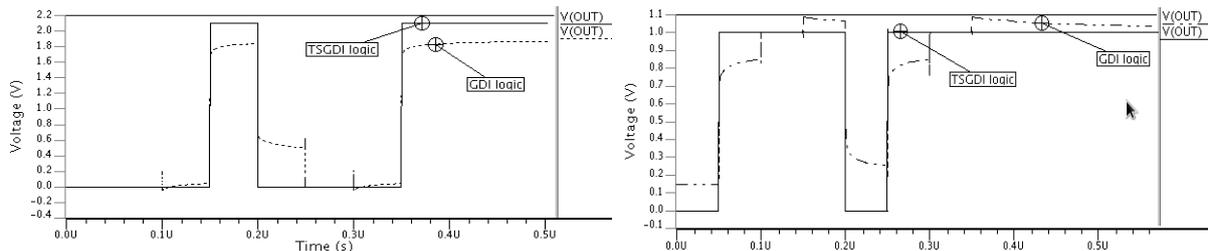
Fig. 3 output of (a) OR gate (b) AND gate using GDI and TSGDI logics

Table.1 Implementation of AND, OR gates and their comparisons results using CMOS, GDI, FSGDI, TSGDI logics

S.NO	Function	Parameter	CMOS logic	GDI logic	FS GDI logic	TS GDI logic
1	AND	Power dissipation (nW)	12.7247	0.02178	15.9636	14.8834
		Delay (pS)	100.82	4.0721	169.14	26.936
		#Tr	6	2	6	6
2	OR	Power dissipation (nW)	30.7108	0.040869	40873.7	30.7303
		Delay (pS)	29.274	3.7812	123.09	25.670
		#Tr	6	2	6	6

The GDI logic consumes very less amount of power and also small chip area, but the output voltage swing of the GDI logic is low at some cases. To increase the output voltage swing FSGDI logic is used in the decoder logic, but in this logic a buffer circuit is used at the output section which increases the voltage swing of output. Here, dissipation of power by the circuit is very high and greater than GDI logic, but the output voltage swing is improved. The TSGDI logic improves the voltage swing at output of the decoder circuit without using any buffers at the output. This paper uses TSGDI logic to construct 8 bit BT decoder circuit. Table.1 clearly shows that the TSGDI and CMOS logics have similar results, but TSGDI logic has better response time than CMOS logic.
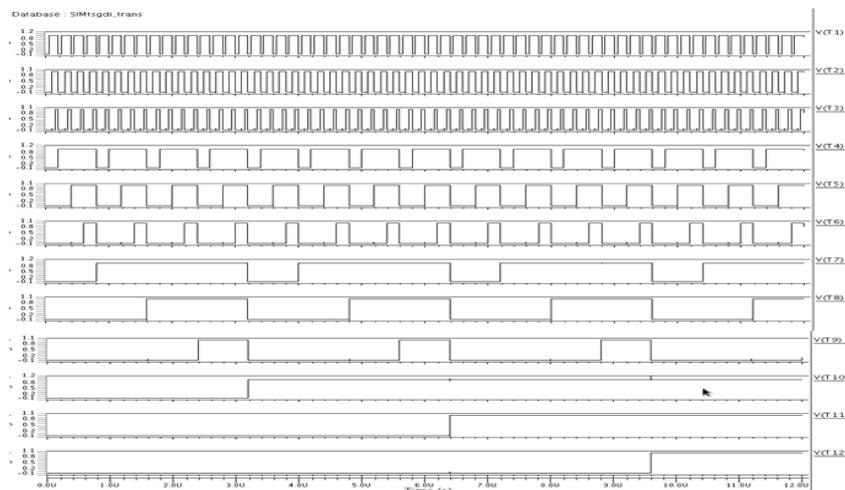
Fig.4 8-Bit Segmented BT Decoder output

The above fig.4 corresponds to the proposed 8 bit BT-decoder circuit which controls the logic of the DAC circuit. Unlike the other decoder circuits the proposed decoder occupies low chip area. To produce 4mV of output voltage a conventional BT decoder circuit produces 0000…..001111(255 bits) code, which means four current sources will be used to produce 4mVof output voltage. In this work the BT-decoder produces 000000001000(12 bits) code to produce 4mV of output voltage, which means only single current source is used in this case. So the number of current sources used in the proposed paper is low, power utilization is more effective.

2.2 Construction of current cell
The current source proposed in this work is shown in below fig.5. The current cell proposed for DAC architecture is designed by taking reduction of power dissipation as main parameter and miniaturization of chip area as another parameter.
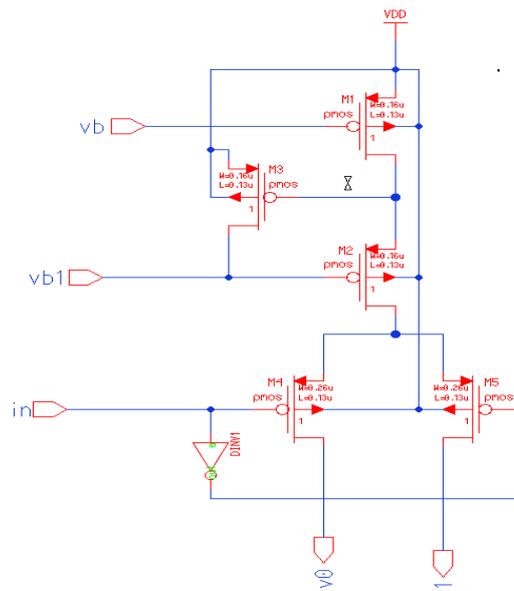
Fig.5 Proposed current source

The current source used in this paper is constructed with the PMOS transistors to reduce the size of the current source cell. Current sources [10] [11] can design with NMOS transistors also, but the area and power requirement is more for those types of architectures. The proposed current cell operation is as follows; transistor M_1 operates in saturation region to produce a reference current value to the current cell. In this proposed CSDAC structure current sources with four (1ImA, 4ImA, 16ImA, 64ImA) different weights is used. These four different weighted current sources are designed by varying the width of the MOS transistor M_1.

The bias voltages V_b, V_{b1} are applied to the transistors M_1, M_2 and M_3 such that all three transistors remain in saturation region. The performance of a current source is depending on output impedance of current source. As the output impedance of the current cell is high the mismatches between current cells are reduces, so that the transistor M_3 is used for increasing the output impedance. The MOS transistors M_4 and M_5 are used as switches in this current cell, which are complementary inputs. The transistors M_4 and M_5 are of every current cell were connected to outputs of the decoder circuit. For example the output of one 2 bit BT decoder is 100, and then one current source is activated and the generated currents through the output resistor R_O. the 8 bit DAC uses twelve current, current signals from every current source is summed at the output load.

The output voltage of DAC is given as

$$V_{out} = I_{out} * R_O \qquad (1)$$

The output current of DAC is give as

$$I_{out} = \quad [(B_1 \vee B_0) + (B_1) + (B_1 \wedge B_0)] (1ImA) + [(B_3 \vee B_2) + (B_3) + (B_3 \wedge B_2)] (4ImA)$$
$$+ [(B_5 \vee B_4) + (B_5) + (B_5 \wedge B_4)] (16ImA)$$
$$+ [(B_7 \vee B_6) + (B_7) + (B_7 \wedge B_6)] (64ImA) \qquad (2)$$

III   Simulation Results

The proposed 8 bit CSDAC architecture in Fig.6 is simulated in 130nm 1P2M CMOS technology with supply voltage 3.3V at the sample rate of 500 MS/s which uses twelve current sources of four different weighted current sources with the values of 1mA, 4mA, 16mA and 64mA connected to the output of the BT decoder circuit. The output of corresponding CSDAC is shown in Fig.6 with the full scale voltage of 255mV. The output of DAC is a staircase with incrimination of 1mV per a step starting from 0mV to 255mV as shown in Fig.7.
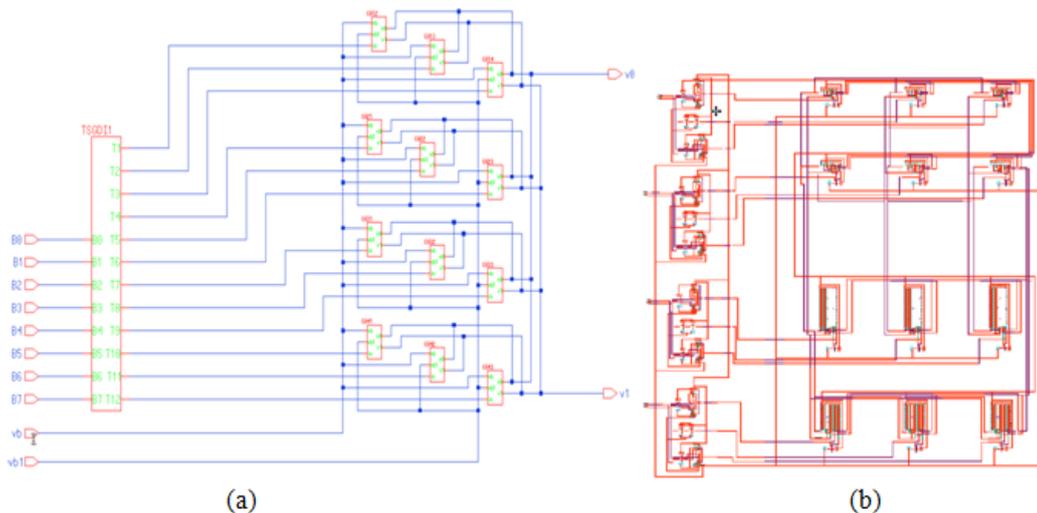
Fig.6 (a) 8-bit CSDAC Schematic and (b) Layout of 8-bit CSDAC
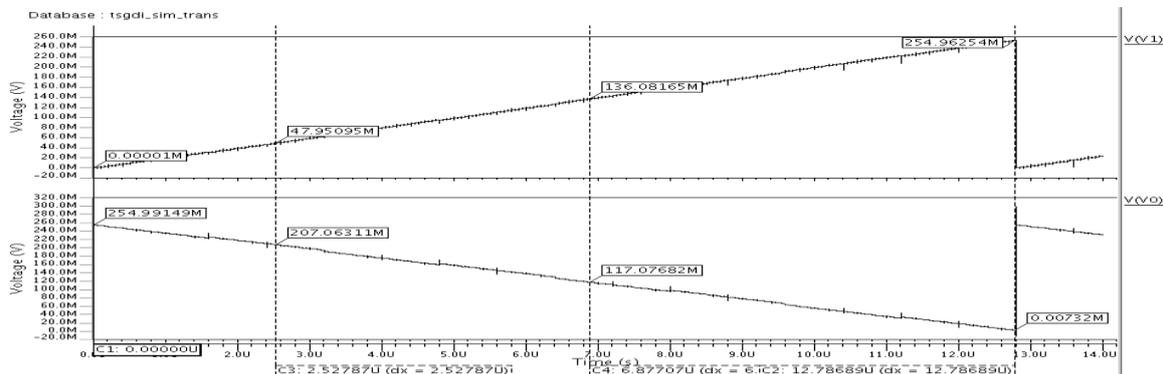
Fig.7 Output of 8-bit Current Steering DAC

Above fig.7 represents output of 8 bit current steering DAC for different input codes, which gives a staircase of ramp signal from 0mV to 255mV by 1mV difference between each step. For example the digital input codes 00000000, 00110000, 10001000, and 11111111; respective output voltages are 0.00001mV, 47.95095mV, 136.08165mV, 254.9625mV. These values are shown V (V_1) waveform in the above fig.7, the other signal V (V_0) is the inverted output waveform of V (V_1).

The total performance of any DAC is defined by the values of INL and DNL errors. If the INL and DNL values of a DAC are less than or equal to ±0.5LSB and ±1LSB respectively then that type of DAC called Monotonic DAC. Differential nonlinearity (DNL) error is defined as the variation of practical output signal step size voltage at each of the input code from 1LSB step. DNL errors cause spurs and additive noise beyond quantization effects. A DNL error beyond ±1LSB can cause Non-Monotonic behavior of a DAC. Integral nonlinearity (INL) is the variation of actual output voltage from ideal output voltage when a straight line drawn between the end points of the transfer function. The DNL and INL of the proposed DAC were ±0.14 LSB and ±0.106LSB, respectively.
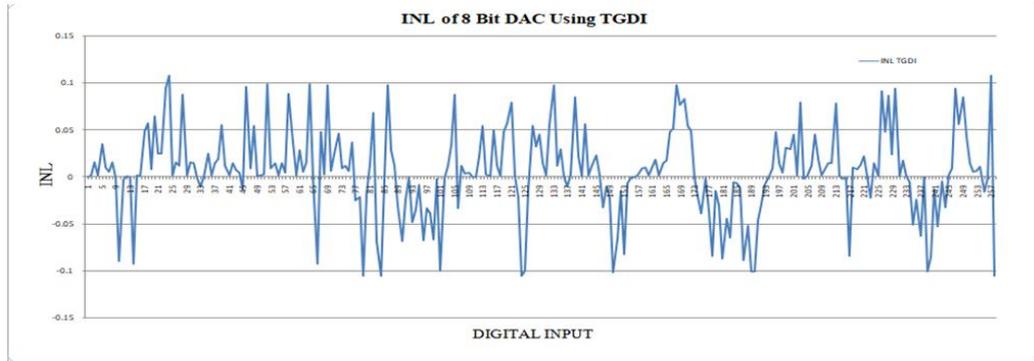
Fig.7 INL of 8-bit CSDAC using TSGDI Logic
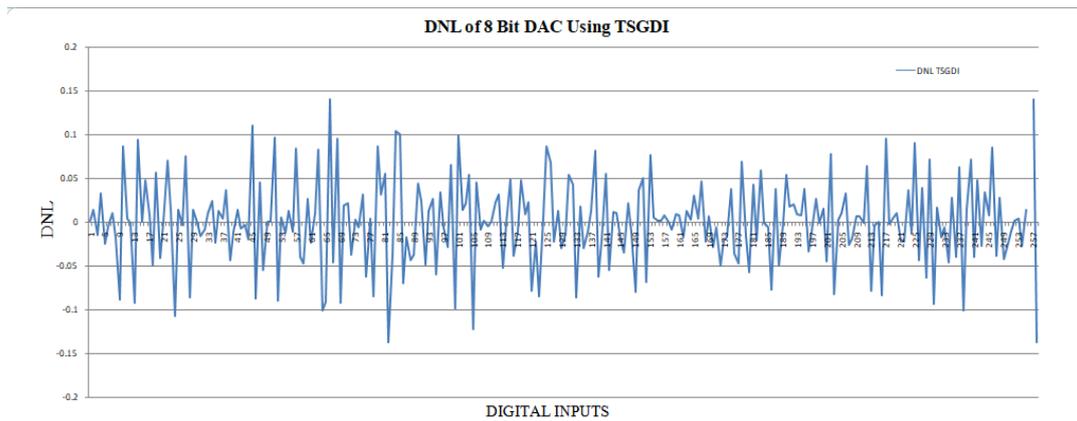
Fig.8 DNL of 8-Bit CSDAC Using TSGDI Logic

Table.2 Implementation results of CSDAC using different GDI logics

Parameter	CMOS Logic	GDI logic	FSGDI	TSGDI(proposed)
Resolution	8 bit	8 bit	8 bit	8 bit
Supply voltage	3.3V	3.3V	3.3V	3.3V
Sample rate	100 MS/s	500 MS/s	500 MS/s	500 MS/s
Full scale voltage	255	255	255	255
Technology	130nm	130nm	130nm	130nm
#Tr	148	116	148	148
DNL	+0.2287/-0.2496LSB	+0.361/-0.3406LSB	+0.2240/-0.2419LSB	+0.14/-0.1367LSB
INL	+0.2044/-0.2915LSB	+0.3072/-0.2958LSB	+0.1910/-0.2097LSB	+0.1079/-0.1056LSB
Power dissipation	30.57 mW	16.7887 mW	36.9520 mW	16.689mW
Area	0.026mm^2	0.0055mm^2	0.00697mm^2	0.00580mm^2

IV   Conclusion

An 8 bit Current steering DAC is implemented in this paper using transmission gate GDI logics with 130nm CMOS technology. The power dissipation of proposed CSDAC is about 16.689mW at sample rate of 500MHz operating at 3.3V supply voltage. The performance of a Current steering DAC is defined by the INL and DNL values. The INL and DNL values of the proposed current steering DAC is +0.1079/-0.1056LSB and +0.14/-0.1367LSB respectively. The chip area occupied by the proposed CSDAC is 0.00580m^2. Table.2 shows that proposed CSDAC got better performance, low chip area, INL and DNL when compared with other models. It is suitable for low chip area and power DAC applications, especially designed for portable devices.

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